REMARKS

I. Introduction

Claims 1 to 8 are currently pending in the present application. Claims 1 and 5 have been amended. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration of the present application is respectfully requested.

II. Rejection of Claims 1 to 8 Under 35 U.S.C. § 103(a)

Claims 1 to 8 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,567,335 ("Norman"). Applicants respectfully submit that Norman does not render unpatentable the present claims for the following reasons.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish *prima facie* obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). It is respectfully submitted that Norman et al. do not disclose or suggest all of the features recited in independent claim 1 or independent claim 5.

Claim 1 has been amended to recite, *inter alia*, "a first buffer memory . . . to which . . . , in the case of a program command access, at least one command following the accessed command is written, wherein a first information line associated with the first buffer memory is used for command transfer, and wherein the accessed command and the at least one command following the accessed command are stored in sequential memory locations of the first buffer memory; and a second buffer memory to which . . . at least one datum following the accessed datum is written, wherein a second information line associated with the second buffer memory is used for data transfer, and wherein the accessed datum and the at least one datum following the accessed datum are stored in sequential memory locations of the second buffer memory; and wherein the at least one command following the accessed command and the at least one datum following the accessed datum are associated with one

another by corresponding sequential positions of the at least one command within the first buffer memory and the at least one datum within the second buffer memory." Claim 5 has been amended to recite substantially similar features as the above-recited features of claim 1.

As recited in amended claims 1 and 5, the present invention substantially reduces the search time for finding a data associated with a particular program command (instruction), by loading the particular program command (into a first buffer memory, using a first information line) and the associated data (into a second buffer memory, using a second information line) in corresponding sequential positions. (See, e.g., Specification, p. 4, l. 5-8). As an example, if three sequential program commands I1, I2 and I3 are present, the following sequence occurs: 1) command I1 will be loaded, followed by loading of any data D1 associated with command I1; 2) command I2 will be loaded, followed by loading of any data D2 associated with command I2; and 3) command I3 will be loaded, followed by loading of any data D3 associated with command I3. Accordingly, a particular program command (instruction) and an associated data are associated with one another by corresponding sequential positions within the respective first and second buffer memories. In this manner, the present invention substantially reduces the conventional search time for finding a data associated with a particular command, since the sequential position automatically provides the association between the command and the connected data.

In contrast to the invention recited in amended claims 1 and 5, the disclosure of Norman does not involve command (instruction) access; instead, Norman merely discloses a memory controller strategy for data reading, which strategy involves address mapping and cache in connection with tag information. In particular, Norman discloses selective reading of data from either a memory device or the control register depending on the tag data, there is simply no program command (instruction) access in the disclosure of Norman. The "commands" mentioned in Norman refers to the commands issued by the memory controller for the memory operation manager, but these commands have nothing to do with the "program command access" recited in claims 1 and 5. Norman indicates that when a special Tag is present on a Tag bus (40), a respective output on a data bus (42) is generated, i.e., the "commands" on bus (40) directly control the data flow as to address mapping and memory control, e.g., in col. 6, lines 15-22, it is stated that when a Tag (19h) is present on the Tag bus (40), data is read out of the device, and when a Tag (1a) is on the Tag bus (40), the contents of a control register are read out of the device. Thus, these "commands" merely control data flow. Taken as a whole, in contrast to the claimed subject matter, Norman merely discloses a conventional memory control strategy in which, if there is a jump command, associated data

is written. In particular, if a special Tag is provided, a corresponding reaction in buffer (52) is established.

Independent of the above, with respect to the command access recited in claims 1 and 5, while the sections of Norman cited in the Office Action may discuss an input buffer (48) to which is connected a Tag Bus (40) via which a Controller (36) may transfer control information, Norman simply does not disclose that during a command access to receive in the input buffer (48) a command, at least one following command is written to the input buffer (48). Similarly, with respect to the data access recited in claims 1 and 5, while the sections of Norman cited in the Office Action may discuss a buffer (52) to which data from Memory Devices (38) are written in accordance with the presence of a Tag written to the input buffer (48), Norman simply does not disclose that during a data access by the Controller (36) via a Tag to receive data from the Memory Devices (38), at least one following datum is written to the buffer (52).

For at least these reasons, it is respectfully submitted that Norman does not render unpatentable claims 1 and 5, as well as their dependent claims 2-4 and 6-8.

In view of the foregoing, withdrawal of this rejection is respectfully requested.

III. Conclusion

In light of the foregoing, it is respectfully submitted that all of the presently pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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